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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,269	07/25/2003	Hong-Yi Hubert Chen	MP0357	7592
26703	7590	03/27/2006	EXAMINER	
HARNESS, DICKEY & PIERCE P.L.C. 5445 CORPORATE DRIVE SUITE 400 TROY, MI 48098			PATEL, HETUL B	
			ART UNIT	PAPER NUMBER
			2186	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/627,269

Applicant(s)

CHEN ET AL.

Examiner

Hetul Patel

Art Unit

2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 and 14-74 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 and 14-74 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. This office action is in response to the communication filed on March 09, 2006. Claims 1 is amended and claims 2-12 and 14-74 are again presented for examination.
2. Claim 13 is missing.
3. Applicant's arguments filed on March 09, 2006 have been fully considered but they are not deemed to be persuasive.
4. The rejection of claims 1-12 and 14-74 as in the previous Office Action is respectfully maintained and reiterated below for Applicant's convenience.

### ***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1 and 5-7 are provisionally rejected under the judicially created doctrine of double patenting over claims 1 and 11-13 of copending Application No. 10/666,892.

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This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows:

10/627,269	10/666,892
Claim 11, 14, 69	Claim 1
Claim 5, 18	Claim 11
Claim 6, 19	Claim 12
Claim 7, 20	Claim 13

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

This is a provisional obviousness-type double patenting rejection.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 8-12, 14-18, 21-26 and 49-74 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaggar (USPN: 5,701,493).

As per claim 1, Jaggar teaches a register file for a data processing system comprising a memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode); input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs for addressing at least one register using an encoded address; and output ports (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from at least one register addressable by an encoded address (e.g. see the abstract and Figs. 1 and 8).

As per claim 2, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) identifies a general purpose register (i.e. registers R0-R13 in Figs. 1 and 8) associated with a processor mode (i.e. a user mode and system mode) (e.g. see the abstract and Figs. 1 and 8).

As per claim 3, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each register (i.e. R0-R15 in Fig. 8) is associated with a register index (i.e. 0000-1111, 17 in Fig. 8) that maps to an encoded address (i.e. the

combination of register address and the mode bits, 17 in Figs. 1 and 8) based on at least one processor mode (i.e. a user mode and system mode) (e.g. see Figs. 1 and 8).

As per claim 4, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the input ports (i.e. the "reg add", mode bits input to 17 and input to 8 in Fig. 8) receive at least one source register index input (i.e. the register address input) and processor mode input (i.e. the mode bits input) for use in providing an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing at least one register (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8).

As per claim 5, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the register file further comprising an address encoder (i.e. the combination of components 12-20 in Fig. 8) to provide an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing one of the plurality of registers (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8).

As per claim 8, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that data for one or more instructions being processed is outputted from the memory unit (i.e. the MMU 62 in Fig. 8) (e.g. see Fig. 8).

As per claim 9, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the register file further comprising input ports (i.e. the "reg add", mode bits input to 17 and input to 8 in Fig. 8) to receive at least one write index input (i.e. the register address input) and processor mode input (i.e. the mode bits input) for use in providing the encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for writing data to at least one register (i.e. to R0-R15 in

Fig. 8); and at least one write input port (i.e. input port to the read buffer 8 shown in Fig. 8) for writing the data to the register (i.e. R0-R15 in Fig. 8) addressable by the encoded address (e.g. see Fig. 8).

As per claim 10, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that data for one or more executed instructions (i.e. instructions/commands buffered in instruction register 12 in Fig. 8) for the data processing are written into the memory unit (i.e. MMU 62 in Fig. 8) (e.g. see Fig. 8).

As per claim 11, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the processor mode includes exception handling modes (i.e. a plurality of IRQ32 etc.) (e.g. see the abstract).

As per claim 12, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the exception handling processor modes include the interrupt request (IRQ) mode (i.e. IRQ32), the fast interrupt request (FRQ) mode (i.e. FRQ32), the undefined instruction (UND) mode (i.e. Undef32) and the abort exception (ABT) mode (i.e. Abt32) (e.g. see the abstract and Col. 2, lines 45-58).

As per claims 14-18 and 21-25, see arguments with respect to the rejection of claims 1-5 and 8-12, respectively. Claims 14-18 and 21-25 are also rejected based on the same rationale as the rejection of claims 1-5 and 8-12, respectively.

As per claim 26, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each exception handling mode corresponds to one or more registers (e.g. see Col. 2, lines 45-58).

As per claim 49, Jaggar teaches a microprocessor comprising an integrated circuit comprising a memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode); and at least one address encoder (i.e. the combination of components 12-20 in Fig. 8) to provide at least one encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for addressing at least one of the plurality of registers (i.e. R0-R15 in Fig. 8) (e.g. see the abstract and Figs. 1 and 8).

As per claims 50-53 and 55, see arguments with respect to the rejection of claims 2-3, 11-12 and 9, respectively. Claims 50-53 and 55 are also rejected based on the same rationale as the rejection of claims 2-3, 11-12 and 9, respectively.

As per claim 54, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that at least one input (i.e. the "reg add", mode bits input to 17 and input to 8 in Fig. 8) to receive index (i.e. the register address input) and processor mode information (i.e. the mode bits input) for use in providing the encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing at least one register (i.e. R0-R15 in Fig. 8); and at least one output (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output

data stored in the storage location (i.e. from the register) addressable by the encoded address (e.g. see Figs. 1 and 8).

As per claim 56, Jaggar teaches a data processing system comprising a memory mapped register file for accessing a plurality of registers (i.e. memory locations) using an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode) (e.g. see the abstract and the Figs. 1 and 8).

As per claims 57 and 63, see arguments with respect to the rejection of claims 49 and 54, respectively. Claims 57 and 63 are also rejected based on the same rationale as the rejection of claims 49 and 54, respectively.

As per claims 58-62 and 64, see arguments with respect to the rejection of claims 2-3, 11-12 and 9, respectively. Claims 58-62 and 64 are also rejected based on the same rationale as the rejection of claims 2-3, 11-12 and 9, respectively.

As per claim 65, Jaggar teaches an integrated circuit method comprising configuring the integrated circuit to receive processor mode (i.e. a user mode and system mode) and source data inputs (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8); configuring the integrated circuit to determine an encoded address based on the processor mode and source data inputs, wherein the encoded address corresponds to a respective one of a plurality of registers (i.e. memory locations) and a corresponding processor mode (i.e. a user mode and system mode);

configuring the integrated circuit to address one of the registers using an encoded address; and configuring the integrated circuit to output data from the register addressable by the encoded address (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) (e.g. see the abstract and Figs. 1 and 8).

As per claim 66, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches about configuring the integrated circuit to output data for multiple instructions (i.e. via the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8).

As per claim 67, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches about configuring the integrated circuit to write data to one of the registers addressable by an encoded address (e.g. see the abstract).

As per claim 68, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches about configuring the integrated circuit to write data to one of the registers for multiple executed instructions (i.e. via the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8).

As per claims 69-74, see arguments with respect to the rejection of claims 1, 65, 65 and 66-68, respectively. Claims 69-74 are also rejected based on the same rationale as the rejection of claims 1, 65, 65 and 66-68, respectively.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 6-7 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar in view of Meier et al. (USPN: 6,363,471) hereinafter, Meier.

As per claims 6 and 7, Jaggar teaches the claimed invention as described above, but failed to teach a latch circuit and a selector as claimed. Meier, however, teaches about using the latch or other clocked storage devices to store the intermediate values for pipelining to the next stage (e.g. see Col. 16, lines 21-35 and Fig. 6). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Meier's latch circuit in the register file taught by Jaggar. In doing so, this latch circuit can buffer the data (i.e. the encoded addresses) for pipeline storage in case if the data can be reused. The further limitation of having the selector coupled to the latch and the address encoder is well-known and notorious old in the art at the time of the current invention was made. By using the selector, such as a mux, the encoded address can be selected either from the latch circuit or directly from the address encoder based on a select signal.

As per claims 19-20, see arguments with respect to the rejection of claims 6-7, respectively. Claims 19-20 are also rejected based on the same rationale as the rejection of claims 6-7, respectively.

8. Claims 27-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar in view of Kerr et al. (USPN: 2003/0159021) hereinafter, Kerr.

As per claim 27, Jaggar teaches a data processing system comprising a microprocessor (i.e. 62 in Fig. 8) comprising a register file, the register file including a memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode); input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs for addressing at least one register using an encoded address; and output ports (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from at least one register addressable by an encoded address (e.g. see the abstract and Figs. 1 and 8).

However, Jaggar does not teach that the microprocessor comprising a plurality of pipeline stages. Kerr, on the other hand, teaches the microprocessor (i.e. the TMC core, 600 in Fig. 6) comprising a plurality of pipeline stages (i.e. 610, 620, 630 and 660 in Fig. 6) (e.g. see paragraph [0003] and Fig. 6). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the plurality of pipeline stages taught by Kerr in the data processing system of Jaggar. In doing so, a number of instructions are being executed in parallel and as a result of that the overall performance of the data processing system increases.

As per claim 28, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the encoded address (i.e. the

combination of register address and the mode bits, 17 in Figs. 1 and 8) identifies a general purpose register (i.e. registers R0-R13 in Figs. 1 and 8) associated with a processor mode (i.e. a user mode and system mode) (e.g. see the abstract and Figs. 1 and 8).

As per claims 29, 31 and 32, the combination of Jaggar and Kerr teaches the claimed invention as described above and furthermore, Kerr teaches that the pipeline stages include an instruction fetch stage (i.e. IF 610 in Fig. 6) to fetch one or more instructions; an instruction decode stage (i.e. ID 620 in Fig. 6) to decode fetched instructions from the instruction fetch stage, the instruction decode stage to forward inputs to the memory unit (i.e. 640 in Fig. 6) for outputting data from or writing data to one or more of the registers (i.e. 652, 654 in Fig. 6), an execution stage (i.e. EX 630 in Fig. 6) including a plurality of execution units (i.e. 646 and 656 in Fig. 6), each execution unit to receive data from the register file for executing an instruction, and a write back or retire logic stage (i.e. WB 660 in Fig. 6) to receive results data associated with one or more instructions executed by the execution units of the execution stage, and to forward the results data to the register file for storage (i.e. via bus 426 in Fig. 6) (e.g. see Fig. 6 and paragraphs [0038]-[0040]).

As per claim 30, the combination of Jaggar and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that the register file further includes a plurality of input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs from the instruction decode stage, the inputs being used to obtain the encoded address for accessing at

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least one register; and at least one output port (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from the register addressable by the encoded address (e.g. see Figs. 1 and 8).

As per claim 33 the combination of Jaggar and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that the register file further includes a plurality of input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive the data from the write back or retire logic for one or more executed instructions, the data to be written in the register file (e.g. see Figs. 1 and 8).

As per claim 34, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each register (i.e. R0-R15 in Fig. 8) is associated with a register index (i.e. 0000-1111, 17 in Fig. 8) that maps to an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) based on at least one processor mode (i.e. a user mode and system mode) (e.g. see Figs. 1 and 8).

As per claim 35, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the processor mode includes exception handling modes (i.e. a plurality of IRQ32 etc.) (e.g. see the abstract).

As per claim 36, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the exception handling processor modes include the interrupt request (IRQ) mode (i.e. IRQ32), the fast interrupt request (FRQ) mode (i.e. FRQ32), the undefined instruction (UND) mode (i.e.

Undef32) and the abort exception (ABT) mode (i.e. Abt32) (e.g. see the abstract and Col. 2, lines 45-58).

As per claim 37, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each exception handling mode corresponds to one or more registers (e.g. see Col. 2, lines 45-58).

As per claims 38-48, see arguments with respect to the rejection of claims 27-37, respectively. Claims 38-48 are also rejected based on the same rationale as the rejection of claims 27-37, respectively.

### ***Remarks***

9. As to the remark, Applicant asserted that with regards to independent claim 1
  - (a) Jaggar does not show, teach or suggest a memory unit having a plurality of registers addressable by an encoded address, wherein the encoded address corresponds to a respective one of the plurality of registers and a corresponding processor mode.
  - (b) FIG. 1 of Jaggar discloses a decoder 17. The decoder 17 receives a composite register address that is a combination of an address from an instruction decoder 14 and a processor mode from a processing status register 18. The decoder 17 compares the composite register address with stored addresses to determine a register address. In contrast, Applicant's invention is directed to registers that are addressable by an encoded address.

- (c) The plurality of registers comprising the memory unit 600 are addressable by an encoded address. Jaggar fails to show, teach, or suggest this structure.
- (d) Jaggar, singly or in combination with Meier or Kerr, does not show, teach, or suggest a memory unit having a plurality of registers addressable by an encoded address, wherein the encoded address corresponds to a respective one of the plurality of registers and a corresponding processor mode.
- (e) It is clear that the Examiner has given little or no consideration of the limitation "a plurality of registers addressable by an encoded address" and failed to give the limitation any weight.
- (f) The registers R0, R1, R2,...R15pc are addressable by the decoded address, and are not addressable by an encoded address because the decoder 17 must first decode the composite register address (Col.4, lines 7-12).

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a), as described above in the rejection of claim 1, Jaggar does teach a memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode) (e.g. see the abstract and Figs. 1 and 8).

With respect to (b)-(e), the decoder 17 in Fig. 1 of Jaggar receives the composite register address that is a combination of a register address (i.e. "reg add" in Fig. 1) from an instruction decoder 14 and a processor mode (i.e. "mode bits" in Fig. 1) from a processing status register 18. Then the decoder 17 compares the composite register address with stored addresses to determine a register address in the memory unit (i.e. the registers RO, R1, R2,...R15pc in Fig. 1) (e.g. see Col. 2, lines 24-33). The instruction decoder (i.e. 14 in Fig. 1) identifies one register within the register bank (i.e. one register from 0000-1111 as shown in Fig. 1), however, one of the register/memory address in the memory unit (i.e. the registers RO, R1, R2,...R15pc in Fig. 1) is later identified by the encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8).

### ***Conclusion***

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MATTHEW KIM  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100